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Romain Cariou, Rosa Ruggeri, Xi Tan, Giovanni Mannino, Joaquim Nassar, et al.. Structural properties of relaxed thin film germanium layers grown by low temperature RF-PECVD epitaxy on Si and Ge (100) substrates. AIP Advances, 2014, pp.077103. 10.1063/1.4886774 . hal-01019905

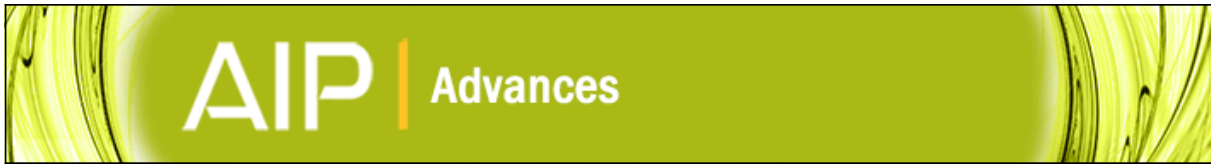
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Citation: [AIP Advances](#) **4**, 077103 (2014); doi: 10.1063/1.4886774

View online: <http://dx.doi.org/10.1063/1.4886774>

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Structural properties of relaxed thin film germanium layers grown by low temperature RF-PECVD epitaxy on Si and Ge (100) substrates

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(Received 2 April 2014; accepted 22 June 2014; published online 1 July 2014)

We report on unusual low temperature (175 °C) heteroepitaxial growth of germanium thin films using a standard radio-frequency plasma process. Spectroscopic ellipsometry and transmission electron microscopy (TEM) reveal a perfect crystalline quality of epitaxial germanium layers on (100) c-Ge wafers. In addition direct germanium crystal growth is achieved on (100) c-Si, despite 4.2% lattice mismatch. Defects rising from Ge/Si interface are mostly located within the first tens of nanometers, and threading dislocation density (TDD) values as low as 10^6 cm^{-2} are obtained. Misfit stress is released fast: residual strain of -0.4% is calculated from Moiré pattern analysis. Moreover we demonstrate a striking feature of low temperature plasma epitaxy, namely the fact that crystalline quality improves with thickness without epitaxy breakdown, as shown by TEM and depth profiling of surface TDD. © 2014 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution 3.0 Unported License. [<http://dx.doi.org/10.1063/1.4886774>]

I. INTRODUCTION

Germanium based electronic devices became an active research topic since the first transistor realization,¹ which opened the path to microelectronics. However, silicon quickly flooded the semiconductor research and industry due to lower cost, abundance and its oxide providing excellent surface passivation. Recently, germanium based electronic devices have gained a renewed interest since silicon device scaling down is rapidly approaching its limit. Due to its higher carrier mobility with respect to Si, Ge has been proposed as a possible candidate for the next generation of high mobility channel devices. From an optical perspective, Ge benefits from high refraction index and minimal optical dispersion, which are useful for lenses and optical elements for infra-red imaging. Thus, improvement in germanium processing, passivation and growth, can impact a lot of different fields: opto-electronics, large area electronics, fiber optics and photovoltaics. In this latter field, germanium is widely used as a bottom cell in record triple junction devices thanks to its strong absorption coefficient together with high mobility and a band gap of 0.66 eV. Moreover, its lattice constant is closely matched to III-V materials.

Driven by the industrial request of cost reduction, research has put aside the conventional wafer technology, moving attention towards new techniques to obtain attractive semiconductor materials on low cost substrates. The main ways to meet this target are crystallization of amorphous materials by novel techniques that allow to preserve the substrate²⁻⁵ or deposition of epitaxial layers, eventually combined with lift off processes for transfer on a flexible support. Within this context, the growth of high quality Germanium with a smooth surface epi-layer on Si is a crucial step for III-V materials

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integration with the existing silicon process technology and it has been a hot research topic for many years.⁶⁻⁹ The main problem arises from the 4.2 % lattice mismatch (at 300K) between Ge and Si which ends up in misfit dislocations and other defects (e.g. twins). Indeed, using buffer layers and specific growth processes, high quality c-Ge can be epitaxially grown on Si using several growth steps involving temperatures above 600°C.^{10,8} However, low temperature deposition is useful for many applications. Among the benefits of low temperature epitaxy we would like to emphasize: i) the absence of thermal strain induced by differences in thermal expansion coefficients; ii) having a hydrogen terminated surface (less reactive), which is a key for low impurity incorporation in non UHV system; and iii) significant cost reduction thanks to well established low temperature plasma CVD reactors.

Here we present our results on thin film epitaxial germanium (epi-Ge) grown by standard RF-PECVD below 200°C. This deposition technique has been widely used for decades to produce amorphous and micro-crystalline materials, but the plasma conditions promoting epitaxial growth at such low temperature is a much more recent result: evidences of Si and Ge epitaxy (up to few tens of nm thick) by RF-PECVD have been reported elsewhere.¹¹⁻¹³ Compared to high temperature CVD epitaxial growth or ultra-high vacuum MBE technique, our approach targets much lower cost. We go here into details about structural properties (stress and defects) of thicker layers, up to 168 nm, of epi-Ge layers on c-Ge and on c-Si substrates, and show that, unlike standard epitaxial techniques,¹⁴⁻¹⁶ low TDD and no epitaxial breakdown is achieved in this approach.

II. EXPERIMENTAL METHOD

Germanium layers were deposited in a standard 13.56 MHz capacitively coupled RF-PECVD reactor,¹⁷ at temperatures from 175 to 200°C. P-type Si (100) and Ge (100) substrates with resistivity below $10^{-2} \Omega \cdot \text{cm}$ were dipped in 5% HF and deionized water ($18.3 \text{ M}\Omega \cdot \text{cm}$) respectively, for oxide removal. Substrates were then immediately loaded into the reactor, with no load-lock chamber, and pumped down to 10^{-7} mbar within 30 min. Reactive species are created from dissociation of a mixture of GeH_4 and H_2 (respectively 5 and 200 sccm) under a RF power density $50 \text{ mW} \cdot \text{cm}^{-2}$ at a total pressure of 2.6 mbar, resulting in a deposition rate of about $5 \text{ \AA} \cdot \text{min}^{-1}$ and thicknesses up to 168 nm. Amorphous hydrogenated silicon (a-Si:H) layers are deposited on top of epitaxial layers, from a silane plasma under a total pressure of 0.13 mbar and RF power density of $6 \text{ mW} \cdot \text{cm}^{-2}$ (deposition rate $0.5 \text{ \AA} \cdot \text{s}^{-1}$). Using the cleaning and growth parameters described above, epi-Ge films covered by a thin aSi:H passivation layer were simultaneously deposited on c-Ge wafers and c-Si wafers. Epi-Ge layers on Ge were first characterized by spectroscopic ellipsometry over the energy range of 1.5–4.5 eV, and fitted using HJY DeltaPsi2 software to determine layers composition and thicknesses. Interface composition, defects and strain were analyzed by transmission electron microscopy, using a JEOL JEM 2010 F TEM microscope operating at an acceleration voltage of 200 kV and equipped with a Gatan electron energy loss image filtering for energy filtered EFTEM analysis, and etching pit density.

III. RESULTS AND DISCUSSION

Figure 1(a) shows the imaginary part of the pseudo-dielectric function of the epi-Ge (circle points) on c-Ge substrate and fitting (red line) with the optical model detailed in inset. The dispersion curve of monocrystalline Ge was used for the epi-Ge layer model, as obtained by Aspnes *et al.*,¹⁸ and a combination of Tauc-Lorentz dispersion formula, large grain polycrystalline silicon (poly-Si) and void for the top a-Si:H layer (Bruggemann approximation). The fit shows excellent agreement on 1.5–4.5 eV range with experimental data, thus confirming that epi-layer is monocrystalline Ge material. However, since no interface layer was found between wafer and epi-layer, which are described by the same material, it was difficult to directly extract epi-Ge thickness from the model. Consequently, a first approximation of Ge deposited thickness was extracted by fitting ellipsometry spectra measured of germanium films co-deposited on crystalline Si wafer and glass substrates. Using

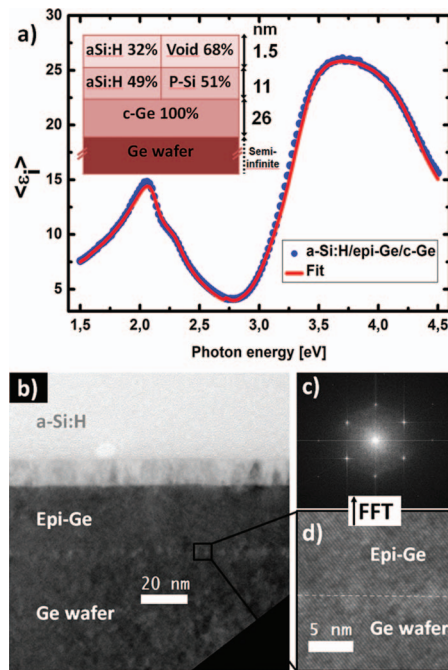


FIG. 1. a) Ellipsometry spectrum of epitaxial germanium on c-Ge wafer, covered by a-Si:H. The red line is the fit of experimental data (circular points) according to the model in the inset. b) HRTEM cross section of the same stack. c) FFT image of epi-Ge/c-Ge interface area enlarged in d).

this procedure our stack was well described by 12.5 ± 0.2 nm of a-Si:H, with a 50% crystalline fraction and 1.5 nm roughness, covering 26 nm of 100 % monocrystalline epi-Ge layer.

These results were correlated with data from TEM, operating at an acceleration voltage of 200 kV, as shown by cross-section micrograph on Figure 1(b). Less than 1 nm discrepancy was observed between the thicknesses deduced from ellipsometry and diffraction contrast TEM micrographs, thus confirming that Ge homoepitaxy thickness can be accurately deduced from fitting ellipsometry data of co-deposited Ge on c-Si and glass substrate. It is interesting to note that a simple deionized water cleaning process of Ge wafer surface results in a very good structural interface, as visible by high resolution TEM [Figure 1(d)]. This is in good agreement with the absence of an interface layer between epi-Ge and c-Ge found by ellipsometry. Further proof of excellent crystal quality is visible from atom periodicity and Fast Fourier Transform (FFT) of the interface showing sharp points [Figure 1(c)]. The 50% crystallinity top mixed phase a-Si:H/p-Si deduced from optical modeling is explained by pyramidal shape epitaxial regrowth inside the a-Si:H layer. This phenomena of epitaxial growth at interface between crystalline material and amorphous phase has been already extensively studied in the case of c-Si/aSi:H heterojunction solar cells,^{19,20} and can be controlled by appropriate interface plasma treatments. Thus, ellipsometry data are fully consistent with TEM analysis and they together constitute the evidence of high quality Ge epitaxy by PECVD achieved at 175°C.

We have then extended this approach to hetero-epitaxy of Ge on c-Si. Layers were deposited at 200°C and both ellipsometry and diffraction contrast TEM cross section view, were used to characterize the epi-Ge layer on c-Si substrate. Figure 2(a) shows the optical model deduced from ellipsometry: the total film thickness is 168 nm with the epi-Ge/air interface described by a 3.8 nm of mixed c-Ge, GeO₂ and voids layer. Accurate data fitting requires to use Si_{1-x}Ge_x alloy for the first 48 nm, with $x = 0.95$, and 100% crystalline germanium for the last 116 nm. To confirm the presence of Si inside germanium layer, suggested by ellipsometric modeling, we have performed energy dispersive X-ray spectroscopy (EDX) on the same sample: we found about 8% of silicon, which is in good agreement with the previous value. As the Ge deposition is performed in a plasma reactor otherwise mostly dedicated to silicon, contamination from silicon residues on the reactor

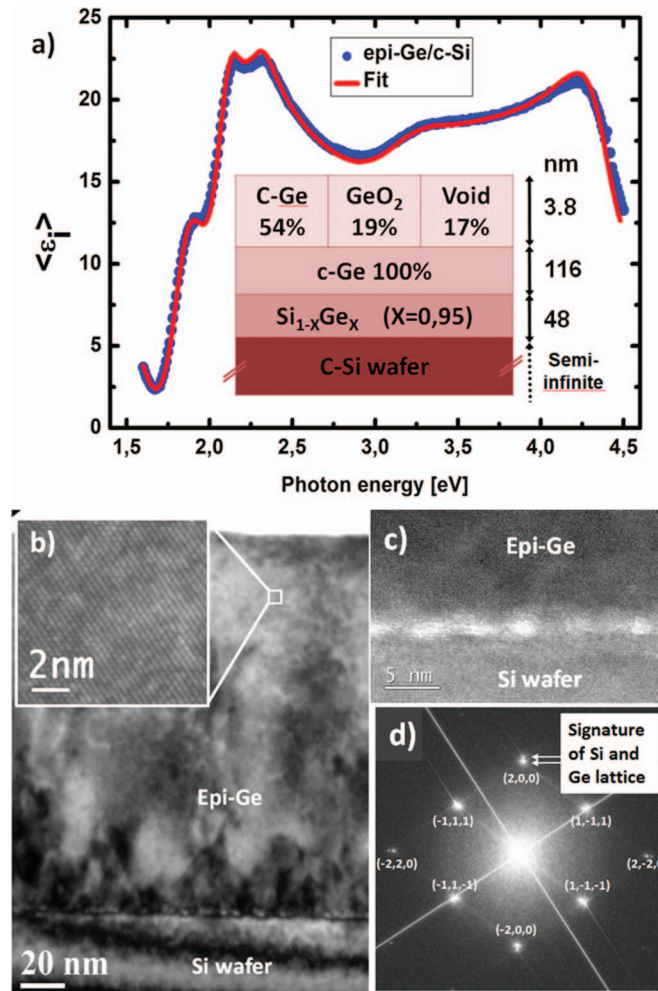


FIG. 2. a) Ellipsometry spectrum of a 168 nm thick epitaxial germanium layer on a c-Si wafer. The red line is the fit of the experimental data (circular points) according to the model in the inset. b) Cross-section TEM picture of the same epitaxial Ge with a high resolution zoom on Ge bulk far from substrate interface. c) Electron filtered TEM image acquired at the wafer interface. White spots are the silicon oxide islands, characterized by a plasmon electron energy loss centered at 26 eV. Inset d) shows FFT of the whole stack with double pattern corresponding to relaxed Ge grown on c-Si wafer.

walls is likely. If desired, appropriate cleaning and pre-coating of the chamber walls should allow a significant reduction of this Si incorporation. However, Si incorporation in epi-Ge film has the beneficial effect of smoothing the structural transition. The lattice parameter for SiGe alloys is given by:²¹

$$a_{\text{Si}_{1-x}\text{Ge}_x} = 0.5431 + 0.01992x + 0.0002733x^2 \text{ nm} \quad (1)$$

In the case of 5–8% Si in Ge, it gives a lattice parameter in the range of [0.5610–0.5616] nm, as compared to 0.5657 nm for bulk Ge, that is [−0.72, −0.83] % of mismatch with respect to Ge. Thus, a better and controlled SiGe graded alloy from interface should contribute to reduce even further defects in Ge layers. TEM cross section analysis was performed to investigate the crystal structure of the layer: on Figure 2(b) it is possible to recognize two regions characterized by different crystal quality:

- (i) A high concentration of dislocations and stacking faults is lying in the first ~50 nanometers, arising from the 4.2% mismatch between Si and Ge lattice. Figure 2(c) shows an EFTEM image acquired at the wafer interface. White spots in the micrographs are the silicon oxide islands, characterized by plasmon electron energy loss centered at 26 eV, remaining after

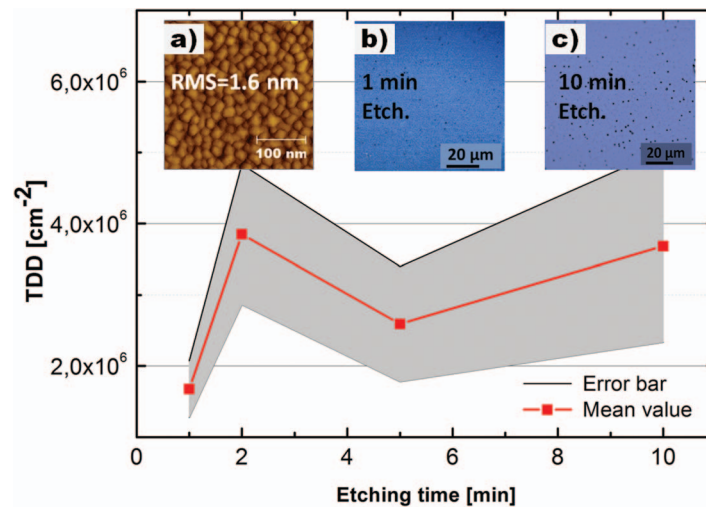


FIG. 3. Depth profile of surface threading dislocation density (TDD), for epi-Ge on c-Si, with iodine etching time. a) AFM image of a 168 nm thick Ge on Si prior etching. Optical images of Ge after b) 1 min and c) 10 min chemical etching for TDD counting.

imperfect cleaning. As a matter of fact, we systematically observe a higher concentration of impurities (O, C, H) in the early stages of depositions, owing to the fact that we use a non UHV environment.^{22,23}

- (ii) A clear improvement in layer crystalline quality with increasing epitaxial thickness: close to the surface very few defect are visible, as testified by inset zoom in Figure 2(b).

The above results indicate that the defective area near the interface with the substrate releases the strain, and germanium adopts its own lattice parameter for the thicker epitaxial growth.²³ This is confirmed by the FFT [see Figure 2(d)]: double pattern for each point is distinguishable, which is the signature of the two lattice parameters Si and Ge.

Epitaxial Ge on Si is known to follow the Stranski-Krastanov (SK) growth mechanism¹⁶ under a variety of experimental deposition conditions (yet high temperature), in which Ge films remain continuous up to a few monolayers before breaking into high density Ge islands. Our deposition occurs at low temperature (175°C) and in a hydrogen rich environment. From the work of Dentel *et al.* and others^{24–26} it is clear that those two factors suppress the 2D-3D transition of the SK growth; appropriate hydrogen adsorption prevents from island growth whereas too high hydrogen coverage may lead to crystalline-amorphous transition. It is known that hydrogen plays a role on surface mobility, but also on etching of weak bonds that could lead to amorphous growth.²⁷ Detailed study of low temperature PECVD epitaxy mechanism is still needed, but Jonhson *et al.*¹¹ already demonstrated that such epitaxial growth conditions in RF-PECVD reactor involve nanocrystals formation in the plasma which contributes, along with Ge radicals, to the growth. This growth process has been further discussed for the case of Si epitaxy,²⁸ and *ab initio* molecular dynamics simulations show that it is likely that nanocrystals melt by impacting the surface before subsequent epitaxial regrowth.

The surface quality of Ge deposited on Si was examined by AFM in tapping mode, and by measuring the etching pit density (EDP). Wet chemical etching by iodine solution [CH_3COOH (65mL)] HNO_3 (20mL)] HF (10mL)] I_2 (30mg)] is a well-established²⁹ method for measuring surface threading dislocation density (TDD) on Ge/Si systems. The surface was found to be relatively flat, with a RMS roughness of 1.6 nm as shown in Figure 3(a), and TDD in the range of $[1.0 \times 10^6 - 6.0 \times 10^6] \text{ cm}^{-2}$ were found for 100 nm thick layers. Those values compare favorably with epitaxial Ge layer produced by chemical vapor deposition in the range of 400 to 600 °C followed by a post-growth anneal at 825 °C.¹⁰ Figure 3 shows the TDD versus etching time with corresponding optical microscope images of Ge surfaces after 1 minute [Figure 3(b)] and 10 min [Figure 3(c)]. We observe

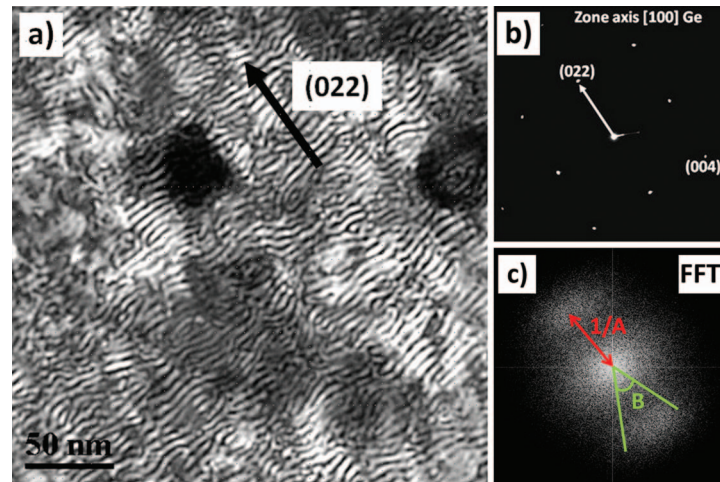


FIG. 4. a) Plan-view TEM of epitaxial germanium on c-Si (100); the fringes are the Moiré pattern obtained in two beam condition using the (220) Si reflection, as shown in b). FFT of the Moiré pattern is presented on inset c) where A is the average value of the fringes spacing and the angle B is related to the distortions in the crystal.

an initial TDD increase before stabilization around $5.0 \times 10^6 \text{ cm}^{-2}$. This trend is consistent with the two regions deduced from ellipsometry and TEM: with longer etching time deeper defects inside epi-Ge become visible. Thus, longer etching time reveals deeper TDD inside the layer, another proof of epitaxial quality improvement with thickness.

Quantitative strain characterization was based on TEM observation of Moiré patterns. Moiré patterns are produced when two crystals with different lattice parameters overlap and the inter-distance between the fringes in the Moiré patterns is strictly related to those lattice parameters.^{30,31}

Figure 4(a) shows the Moiré pattern (fringes) obtained in two beams bright field configuration, for an epi-Ge/c-Si sample observed in plan-view, choosing one of the (220) directions [Figure 4(b)]. The sample was tilted in such a way that all the reflections around the silicon [100] zone axis were far from the exact Bragg position. This configuration strongly reduces the diffraction contrast arising from defects and allows us to see the Moiré pattern clearly. The non-continuous fringes reveal some complex structure on defects, which needs further investigation. To get quantitative information on lattice parameters we have analyzed the FFT of the image, as Figure 4(c) shows. The average value of the inter-distance fringes A, is deduced from the distance between the center of the FFT and the center of the halo, that is $1/A$ as shown on Figure 4(c); and B is related to the bending of the fringes coming from distortions in the Ge epitaxial domains. Thus, measuring A we are able to know with high accuracy the inter-distance of (220) plane $d_{\text{epi-Ge}(220)}$. Assuming symmetry in the x-y plane for this face-centered cubic system, one can find the lattice parameter $a_{\text{epi-Ge}}$, and the biaxial strain ε :

$$d_{\text{epi-Ge}(220)} = A \times d_{\text{Si}(220)} / (A - d_{\text{Si}(220)}) \quad (2)$$

$$a_{\text{epi-Ge}} = d_{\text{epi-Ge}} \times (h^2 + k^2 + l^2)^{1/2} \quad (3)$$

$$\varepsilon = (a_{\text{epi-Ge}} - a_{\text{Ge}}) / a_{\text{Ge}} \quad (4)$$

For a perfect crystal, one can find in literature $d_{\text{Si}(220)} = 0.1919 \text{ nm}$ and $a_{\text{Ge}} = 0.5657 \text{ nm}$; with the experimental value $A = 5.221 \pm 0.074 \text{ nm}$ (error introduced by pixel size) we finally get $\varepsilon = -0.39 \pm 0.06 \%$. This confirms that despite the 4.2% mismatch between those two crystals, there is a good relaxation of epi-Ge crystal grown on c-Si wafer. Besides, the non-zero value and the negative symbol of ε reveal a slightly compressively residual strain.

IV. SUMMARY AND CONCLUSIONS

We demonstrated epitaxial germanium growth by standard RF-PECVD at 200°C on both c-Ge and c-Si substrates. Investigation of the material quality by means of ellipsometry, TEM, AFM and chemical etching has proven the high crystalline quality of the layers. Supported by HRTEM analyses, we have shown that appropriate ellipsometry data fitting can provide accurate determination of the layers thickness, composition, and interfaces quality. Excellent structural quality epi-Ge on c-Ge has been grown by this simple low temperature process. For epi-Ge on c-Si substrate, stacking faults arising from the Si and Ge mismatch, as well as Si contamination, are located in the first tens of nanometers above interface, and then crystal quality improves with thickness. Less than 200 nm of epi-Ge are needed to achieve low roughness and low surface threading dislocation density. From Moiré patterns analysis, we found a low residual slightly compressively strain in the range of -0.4% . These results, in particular the excellent quality of the heteroepitaxial Ge layers open the way to various applications in optoelectronics.

ACKNOWLEDGMENTS

The authors would like to acknowledge Jean-Luc Maurice and Guillaume Courtois for helpful discussions and critical reading.

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